

NuMicro™ Series NM1510/520/530 Preliminary Product Brief

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1 GENERAL DESCRIPTION

The NuMicro™ NM15xx Series 32-bit microcontroller is embedded with the newest ARM® Cortex™-M0 core at a cost equivalent to traditional 8-bit microcontroller for industrial control and applications which need high performance.

The NuMicro™ NM15xx Series embedded with the Cortex™-M0 core runs up to 72 MHz and supports a variety of industrial control and applications which need high CPU performance. The NuMicro™ NM15xx Series provides 128K/64K/32K bytes embedded flash, 4 Kbytes data flash, 4 Kbytes flash for the ISP, and 16K/8K/4K bytes embedded SRAM. This MCU includes advanced PWM function, MDU (motor drive unit) and input capture timer which are specially designed for motor driving application. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer, UART, SPI, I2C, PWM Timer, GPIO, 12-bit ADC, Low Voltage Detector and Brown-out detector. These useful functions make the NuMicro™ NM15xx Series powerful for a wide range of applications.

In addition, the NuMicro™ NM15xx Series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
 - ARM® Cortex™ -M0 core runs up to 72 MHz
 - One 24-bit system timer
 - Supports low power sleep-mode
 - Single-cycle 32-bit hardware multiplier
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Supports Serial Wire Debug (SWD) support with two watchpoints and four breakpoints
- Memory
 - 128K/64K/32K bytes Flash for program memory (APROM)
 - 8 Kbytes Flash memory for ISP loader (LDROM)
 - 4 Kbytes Flash memory for Data Flash
 - Supports In-system program (ISP) and In-application program (IAP) application code update
 - 16K/8K/4K bytes SRAM for internal scratch-pad RAM
 - Supports 2 wire ICP update from ICE interface
 - Supports fast parallel programming mode by external programmer
- Clock Control
 - Programmable system clock source
 - Built-in internal 22.1184 MHz OSC (trimmed to 1%) for system operation
 - Built-in low power 10 kHz OSC for watchdog timer and wake-up in sleep mode
 - External 4~24 MHz crystal input
 - Supports one PLL, up to 72MHz, for high performance system operation
- Hardware divider
 - Supports signed 32-bit dividend, 16-bit divisor operation
- GPIO port
 - Up to 8-bit, 11-port I/O
 - Bit control available
 - Four I/O modes:
 - ◆ Quasi bi-directional
 - ◆ Push-pull (output with high driver and sink current)
 - ◆ Open-drain
 - ◆ Input only with high impedance (default)
 - TTL/Schmitt trigger input selectable
 - I/O pins configurable as interrupt source with edge/level setting
 - INT0 and INT1 pins with individual interrupt vectors
- Timers
 - Supports four channel 32-bit timers; one 8-bit pre-scale counter with 24-bit up-timer for each timer



- 24-bit timer value is readable through TDR (Timer Data Register)
- Supports One-shot, Periodic and Toggle operation modes
- Supports event counter function
- Watchdog Timer
 - ON/OFF by hardware configuration or software
 - Multiple clock sources
 - Supports wake-up from Power-down or Sleep mode
 - Interrupt or reset selectable on watchdog time-out
 - Time-out reset delay period time can be selected
- WWDT (Window Watchdog Timer)
 - 6-bit down counter with 11-bit pre-scale for wide range window selected
- Basic PWM
 - 1 unit of 16-bit basic PWM, up to 2ch output
 - Alternative function as input capture timer
- Enhanced PWM
 - 2 units of 16-bit enhanced PWM, up to 6ch output with dead-zone control, brake and polarity control for motor drive
 - Default tri-state during any reset
- Enhanced Input Capture
 - Up to 2 units of 24-bit input capture
 - Each unit has 3 inputs: IC0, IC1 and IC2
- QEI (Quadrature Encoder Interface)
 - Up to 2 units of Quadrature Encoder Interface
 - Each unit has 3 inputs: QEIA, QEIB and IDX
- MDU (Motor Drive Unit)
 - Built-in PI + FOC + SVPWM
 - Output Space Vector PWM timing to PWM unit 0/1
- UART
 - Up to two 16550 compatible UART devices
 - Programmable baud-rate generator
 - Buffered receiving and transmitting, each with 16 bytes FIFO
 - Supports flow control (TX, RX, CTS and RTS)
 - Supports IrDA(SIR) function
 - Supports RS-485
- SPI
 - Up to three sets of SPI device
 - Supports SPI master/slave mode
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 8 to 32 bits
 - MSB or LSB first data transfer

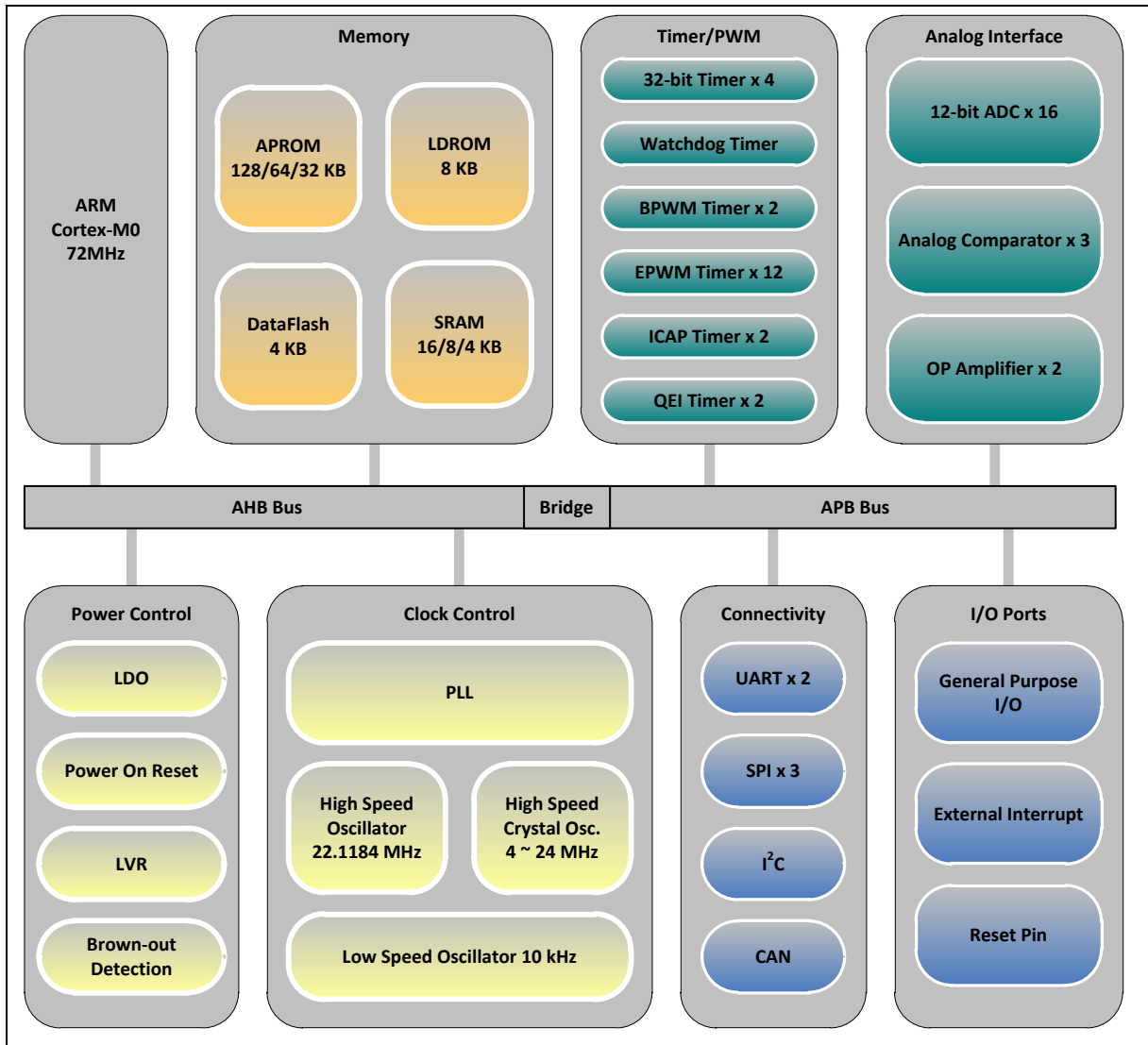


- Rx and Tx on both rising or falling edge of serial clock independently
 - Supports Byte Suspend mode in 32-bit transmission
- I²C
 - Master/Slave up to 1 Mbit/s
 - Bi-directional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters
 - Programmable clocks allow versatile rate control
 - Multiple address recognition (four slave address with mask option)
- CAN
 - CAN 2.0B protocol compatible device
 - Support 11-bit identifier as well as 29-bit identifier
 - Bit rates up to 1Mbits/s
 - NRZ bit Coding/ Encoding
 - Error Detection & Status Report
 - Bit error, Form error, Stuffing error, 15-bit CRC detection, and Acknowledge error Interrupt
 - Bit Timing Synchronization
 - Acceptance filter extension
- ADC
 - Two A/D converters
 - Each ADC with up to 8 channel, 12-bit resolution with 10-bit accuracy
 - 16 result registers
 - Sampling rate up to 800ksps
 - Two operating modes:
 - Single Sampling mode: Only one specified channel can be sampled at one time.
 - Simultaneous Sampling mode: Allowing two ADC channels to be sampled simultaneously.
 - Two converting result digital comparators
 - Conversion start by software, external pins, or linked with Timer 0~3 or PWM module
- Up to three Analog Comparators
- Up to two OPA (operational amplifier)
- Brown-out detector
 - 4 levels: 4.4V/3.7V/2.7V/2.2V
 - Optional brown-out interrupt or reset



- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Low Voltage Reset
- 96-bit unique ID
- Operating Temperature: -40°C ~105°C
- Develop tools: parallel writer or In-Circuit Programming (ICP) writer
- Packages:
 - All Green package (RoHS)
 - LQFP 100/64/48-pin

3 BLOCK DIAGRAM





4 PARTS LIST

| | NM1530VE3AE NM1530VD3AE | NM1520RD2AE NM1520RC2AE | NM1520LD2AE NM1520LC2AE | NM1521RD2AE | NM1510LC1AE |
|-------------------|--|--|---|--|---|
| AP Flash | 128KB/64KB | 64KB/32KB | 64KB/32K | 64KB | 32KB |
| RAM | 16KB | 8KB | 8KB | 8KB | 4KB |
| Data Flash | 4KB | 4KB | 4KB | 4KB | 4KB |
| Timer | 4 x 24-bit | 4 x 24-bit | 4 x 24-bit | 4 x 24-bit | 4 x 24-bit |
| PWM | 6ch PWM0, 6ch PWM1 2ch PWM2 | 6ch PWM0, 6ch PWM1 1ch PWM2 | 6ch PWM0, 3ch PWM1 | 6ch PWM0, 6ch PWM1 1ch PWM2 | 6ch PWM0, 3ch PWM1 |
| QEI IC | 3ch x 2 sets(QEI0,QEI1) 3ch x 2 sets(IC0,IC1) | 3ch x 1 set(QEI0,QEI1) Pin shared with QEI0 | 3ch x 1 set(QEI0) Pin shared with QEI0 | 3ch x 1 set(QEI0) 3ch x 1 set (IC1) | 3ch x 1 set(QEI0) Pin shared with QEI0 |
| UART | 2 | 2 | 2 | 2 | 2 |
| SPI | 3 | 1 | 1 | 1 | 1 |
| I2C | 1 | 1 | 1 | 1 | 1 |
| CAN 2.0B | 1 | 1 | 1 | 1 | - |
| ADC | 8ch ADCA 8ch ADCB | 7ch ADCA 7ch ADCB | 5ch ADCA 4ch ADCB | 4ch ADCA 7ch ADCB | 5ch ADCA 4ch ADCB |
| Comparator | CMP0, CMP1, CMP2 | CMP1, CMP2 | CMP1 | CMP2 | CMP1 |
| OP | OP0, OP1 | OP0, OP1 | OP0, OP1 | OP0, OP1 | OP0, OP1 |
| Package | LQFP100(14x14x1.4mm) | LQFP64(10x10x1.4mm) | LQFP48(7x7x1.4mm) | LQFP64(10x10x1.4mm) | LQFP48(7x7x1.4mm) |

5 PIN CONFIGURATION

5.1 LQFP 100-pin

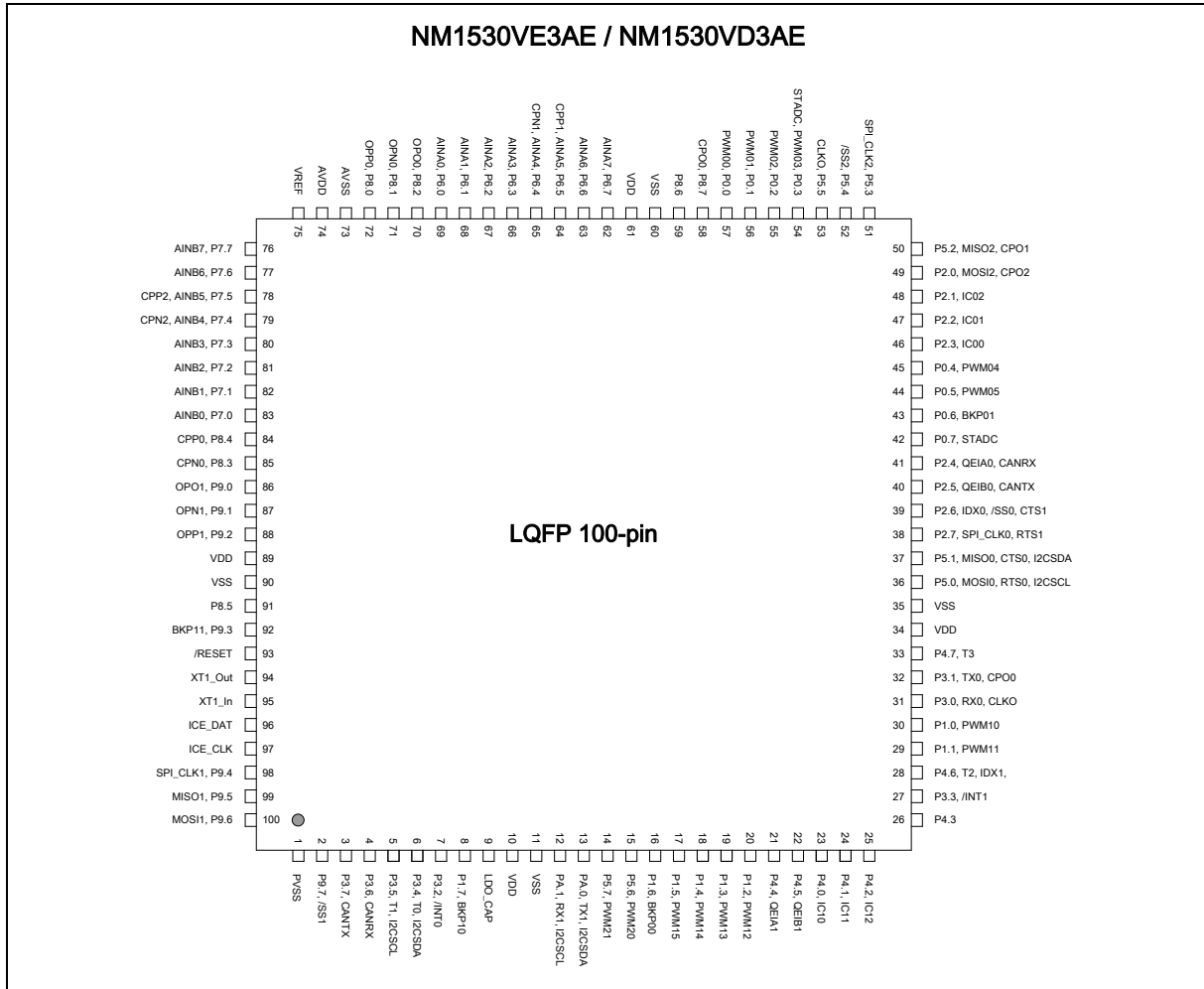


Figure 5–1 NuMicro™ NM15xx Series LQFP-100 Pin Diagram

5.2 LQFP 64-pin

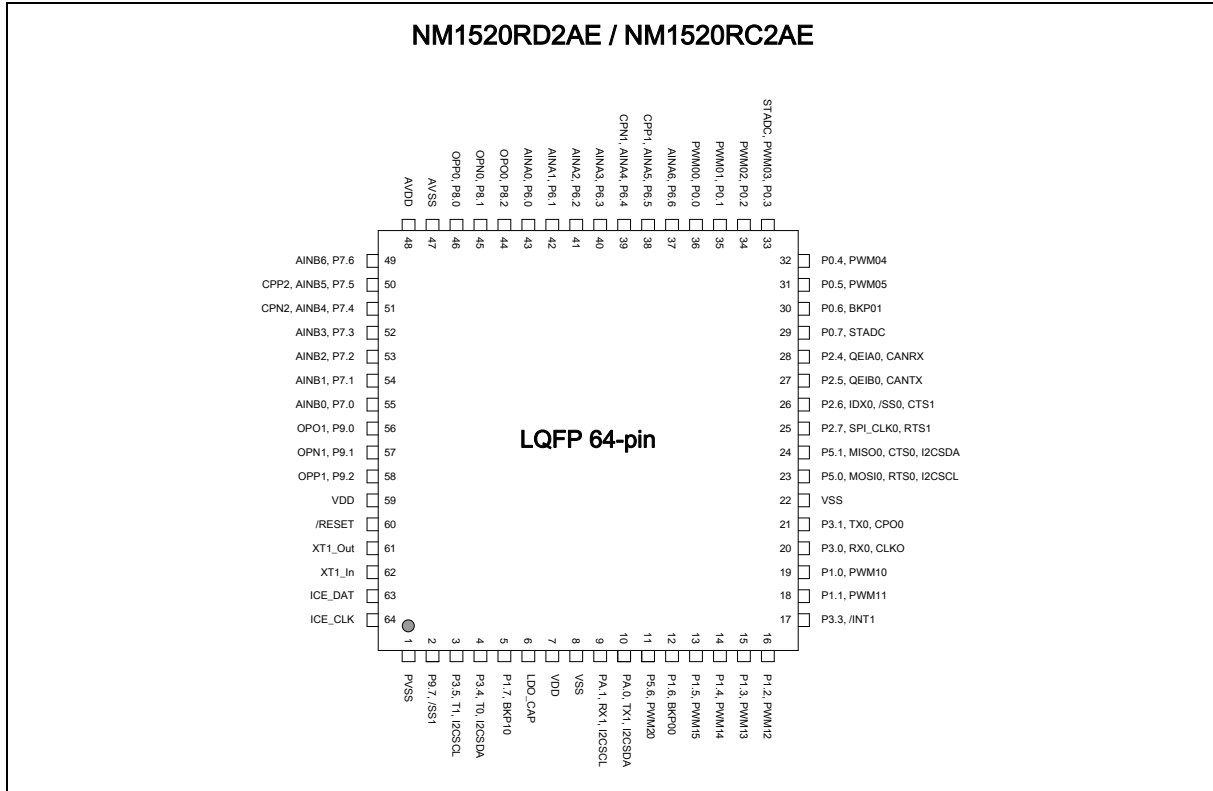


Figure 5–2 NuMicro™ NM15xx Series LQFP-64 Pin Diagram

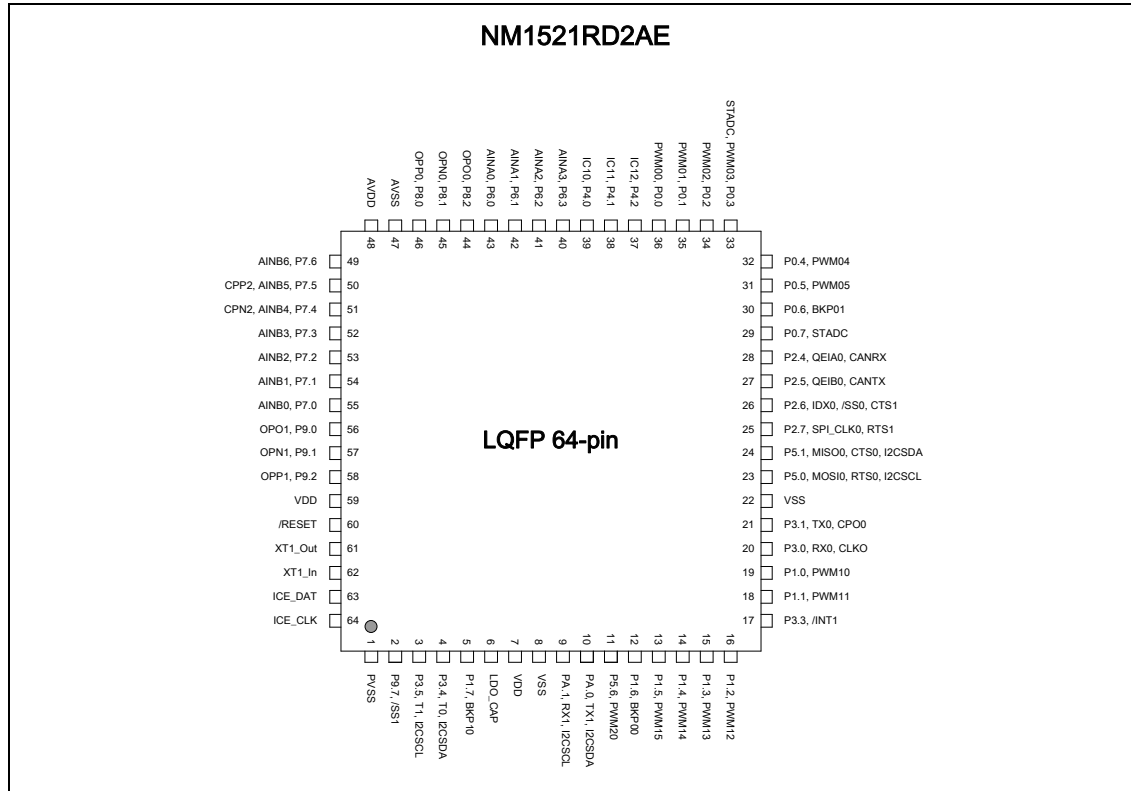


Figure 5–3 NuMicro™ NM1521 Series LQFP-64 Pin Diagram

5.3 Pin Description

| Pin Number | | | Pin Name | Pin Type ^[1] | Description |
|------------|--------|--------|------------------|-------------------------|---|
| 100-pin | 64-pin | 48-pin | | | |
| 10 | 7 | 5 | V _{DD} | P | POWER SUPPLY: Supply voltage Digital V _{DD} for operation. |
| 34 | | | | | |
| 61 | 59 | 5 | V _{DD} | P | POWER SUPPLY: Supply voltage Digital V _{DD} for operation. |
| 89 | | | | | |
| 11 | 8 | 6 | V _{SS} | P | GROUND: Digital Ground potential. |
| 35 | | | | | |
| 60 | 22 | 6 | V _{SS} | P | GROUND: Digital Ground potential. |
| 90 | | | | | |
| 9 | 6 | 4 | LDO_CAP | P | LDO: LDO output pin Note: It needs to be connected with a 10uF capacitor. |
| 1 | 1 | 1 | PVSS | P | PLL GROUND: PLL Ground potential. |
| 74 | 48 | 36 | AV _{DD} | AP | Power supply for internal analog circuit |
| 73 | 47 | 35 | AV _{SS} | AP | Ground Pin for analog circuit |
| 75 | - | - | Vref | AP | Voltage reference input for ADC |
| 93 | 60 | 44 | /RESET | I (ST) | RESET: /RST pin is a Schmitt trigger input pin for hardware device reset. A "Low" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND. |
| 94 | 61 | 45 | XT_OUT | O | CRYSTAL OUT: This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1. |
| 95 | 62 | 46 | XT_IN | I (ST) | CRYSTAL IN: This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default. |
| 96 | 63 | 47 | ICE_DAT | I/O | Serial Wired Debugger Data pin |
| 97 | 64 | 48 | ICE_CLK | I | Serial Wired Debugger Clock pin |
| 57 | 36 | 26 | P0.0 | I/O | General purpose digital I/O pin |
| | | | PWM00 | O | PWM0 output of PWM Unit 0 |
| 56 | 35 | - | P0.1 | I/O | General purpose digital I/O pin |
| | | | PWM01 | O | PWM1 output of PWM Unit 0 |
| 55 | 34 | 25 | P0.2 | I/O | General purpose digital I/O pin |
| | | | PWM02 | O | PWM2 output of PWM Unit 0 |
| 54 | 33 | - | P0.3 | I/O | General purpose digital I/O pin |
| | | | PWM03 | O | PWM3 output of PWM Unit 0 |
| | | | STADC | I | ADC external trigger input |



| Pin Number | | | Pin Name | Pin Type ^[1] | Description |
|------------|--------|--------|----------|-------------------------|--------------------------------------|
| 100-pin | 64-pin | 48-pin | | | |
| 45 | 32 | 23 | P0.4 | I/O | General purpose digital I/O pin |
| | | | PWM04 | O | PWM4 output of PWM Unit 0 |
| 44 | 31 | - | P0.5 | I/O | General purpose digital I/O pin |
| | | | PWM05 | O | PWM5 output of PWM Unit 0 |
| 43 | 30 | - | P0.6 | I/O | General purpose digital I/O pin |
| | | | BKP01 | I | Brake input pin 1 of PWM Unit 0 |
| 42 | 29 | - | P0.7 | I/O | General purpose digital I/O pin |
| | | | STADC | I | ADC external trigger input |
| 30 | 19 | 14 | P1.0 | I/O | General purpose digital I/O pin |
| | | | PWM10 | O | PWM0 output of PWM Unit 1 |
| 29 | 18 | 13 | P1.1 | I/O | General purpose digital I/O pin |
| | | | PWM11 | O | PWM1 output of PWM Unit 1 |
| 20 | 16 | 12 | P1.2 | I/O | General purpose digital I/O pin |
| | | | PWM12 | O | PWM2 output of PWM Unit 1 |
| 19 | 15 | 11 | P1.3 | I/O | General purpose digital I/O pin |
| | | | PWM13 | O | PWM3 output of PWM Unit 1 |
| 18 | 14 | 10 | P1.4 | I/O | General purpose digital I/O pin |
| | | | PWM14 | O | PWM4 output of PWM Unit 1 |
| 17 | 13 | 9 | P1.5 | I/O | General purpose digital I/O pin |
| | | | PWM15 | O | PWM5 output of PWM Unit 1 |
| 16 | 12 | - | P1.6 | I/O | General purpose digital I/O pin |
| | | | BKP00 | I | Brake input pin 0 of PWM Unit 0 |
| 8 | 5 | 3 | P1.7 | I/O | General purpose digital I/O pin |
| | | | BKP10 | I | Brake input pin0 of PWM Unit 1 |
| 49 | - | - | P2.0 | I/O | General purpose digital I/O pin |
| | | | MOSI2 | I/O | SPI2 MOSI (Master Out, Slave In) pin |
| | | | CPO2 | AO | Analog comparator 2 output pin |
| 48 | - | - | P2.1 | I/O | General purpose digital I/O pin |
| | | | IC02 | I | Input 2 of Input Capture Unit 0 |
| 47 | - | - | P2.2 | I/O | General purpose digital I/O pin |
| | | | IC01 | I | Input 1 of Input Capture Unit 0 |
| 46 | - | - | P2.3 | I/O | General purpose digital I/O pin |
| | | | IC00 | I | Input 0 of Input Capture Unit 0 |



| Pin Number | | | Pin Name | Pin Type ⁽¹⁾ | Description |
|------------|--------|--------|----------|-------------------------|---|
| 100-pin | 64-pin | 48-pin | | | |
| 41 | 28 | 22 | P2.4 | I/O | General purpose digital I/O pin |
| | | | QEIA0 | I | Quadrature encoder phase A input of QE1 Unit 10 |
| | | | CANRX | I | CAN Bus RX Input (not supported in 48-pin) |
| 40 | 27 | 21 | P2.5 | I/O | General purpose digital I/O pin |
| | | | QEIB0 | I | Quadrature encoder phase B input of QE1 Unit 0 |
| | | | CANTX | O | CAN Bus TX Output (not supported in 48-pin) |
| 39 | 26 | 20 | P2.6 | I/O | General purpose digital I/O pin |
| | | | IDX0 | I | Quadrature Encoder Index input of QE1 Unit 0 |
| | | | /SS0 | I/O | SPI0 slave select pin |
| | | | CTS1 | I | UART1 CTS pin |
| 38 | 25 | 19 | P2.7 | I/O | General purpose digital I/O pin |
| | | | SPI_CLK0 | I/O | SPI0 serial clock pin |
| | | | RTS1 | O | UART1 RTS pin |
| 31 | 20 | 15 | P3.0 | I/O | General purpose digital I/O pin |
| | | | RX0 | I | Data Receiver input pin for UART0 |
| 32 | 21 | 16 | P3.1 | I/O | General purpose digital I/O pin |
| | | | TX0 | O | Data transmitter output pin for UART0 |
| | | | CPO0 | AO | Analog comparator 0 output |
| 7 | - | 2 | P3.2 | I/O | General purpose digital I/O pin |
| | | | /INT0 | I | External Interrupt 0 input pin |
| 27 | 17 | - | P3.3 | I/O | General purpose digital I/O pin |
| | | | /INT1 | I | External Interrupt 1 input pin |
| 6 | 4 | - | P3.4 | I/O | General purpose digital I/O pin |
| | | | T0 | I/O | Timer0 external clock |
| | | | I2CSDA | I/O | I2C data input/output pin |
| 5 | 3 | - | P3.5 | I/O | General purpose digital I/O pin |
| | | | T1 | I/O | Timer1 external clock |
| | | | I2CSCL | I/O | I2C clock output pin |
| 4 | - | - | P3.6 | I/O | General purpose digital I/O pin |
| | | | CANRX | I | CAN Bus RX Input |
| 3 | - | - | P3.7 | I/O | General purpose digital I/O pin |
| | | | CANTX | O | CAN Bus TX Output |
| 23 | - | - | P4.0 | I/O | General purpose digital I/O pin |



| Pin Number | | | Pin Name | Pin Type ^[1] | Description |
|------------|--------|--------|----------|-------------------------|--|
| 100-pin | 64-pin | 48-pin | | | |
| | | | IC10 | I | Input 0 of Input Capture Unit 1 |
| 24 | - | - | P4.1 | I/O | General purpose digital I/O pin |
| | | | IC11 | I | Input 1 of Input Capture Unit 1 |
| 25 | - | - | P4.2 | I/O | General purpose digital I/O pin |
| | | | IC12 | I | Input 2 of Input Capture Unit 1 |
| 26 | - | - | P4.3 | I/O | General purpose digital I/O pin |
| 21 | - | - | P4.4 | I/O | General purpose digital I/O pin |
| | | | QEIA1 | I | Quadrature encoder phase A input of QE1 Unit 1 |
| 22 | - | - | P4.5 | I/O | General purpose digital I/O pin |
| | | | QEIB1 | I | Quadrature encoder phase B input of QE1 Unit 1 |
| 28 | -- | - | P4.6 | I/O | General purpose digital I/O pin |
| | | | T2 | I/O | Timer2 external clock |
| | | | IDX1 | I | Quadrature Encoder Index input of QE1 Unit 1 |
| 33 | - | - | P4.7 | I/O | General purpose digital I/O pin |
| | | | T3 | I/O | Timer3 external clock |
| 36 | 23 | 17 | P5.0 | I/O | General purpose digital I/O pin |
| | | | MOSI0 | I/O | SPI0 MOSI (Master Out, Slave In) pin |
| | | | RTS0 | O | UART0 RTS pin |
| 37 | 24 | 18 | P5.1 | I/O | General purpose digital I/O pin |
| | | | MISO0 | I/O | SPI0 MISO (Master In, Slave Out) pin |
| | | | CTS0 | I | UART0 CTS pin |
| 50 | - | 24 | P5.2 | I/O | General purpose digital I/O pin |
| | | | MISO2 | I/O | SPI2 MISO (Master In, Slave Out) pin |
| | | | CPO1 | AO | Analog comparator 1 output pin |
| 51 | - | - | P5.3 | I/O | General purpose digital I/O pin |
| | | | SPI_CLK2 | I/O | SPI2 serial clock pin |
| 52 | - | - | P5.4 | I/O | General purpose digital I/O pin |
| | | | /SS2 | I/O | SPI2 slave select pin |
| 53 | - | - | P5.5 | I/O | General purpose digital I/O pin |
| | | | CLKO | O | Frequency Divider output pin |
| 15 | 11 | - | P5.6 | I/O | General purpose digital I/O pin |
| | | | PWM20 | I/O | PWM0 output of PWM unit 2 |
| 14 | - | - | P5.7 | I/O | General purpose digital I/O pin |



| Pin Number | | | Pin Name | Pin Type ⁽¹⁾ | Description |
|------------|--------|--------|----------|-------------------------|--|
| 100-pin | 64-pin | 48-pin | | | |
| | | | PWM21 | I/O | PWM1 output of PWM unit 2 |
| 69 | 42 | - | P6.0 | I/O | General purpose digital I/O pin |
| | | | AINA0 | AI | ADC analog input 0 for sample-and-hold A |
| 68 | 42 | 31 | P6.1 | I/O | General purpose digital I/O pin |
| | | | AINA1 | AI | ADC analog input 1 for sample-and-hold A |
| 67 | 41 | 30 | P6.2 | I/O | General purpose digital I/O pin |
| | | | AINA2 | AI | ADC analog input 2 for sample-and-hold A |
| 66 | 40 | 29 | P6.3 | I/O | General purpose digital I/O pin |
| | | | AINA3 | AI | ADC analog input 3 for sample-and-hold A |
| 65 | 39 | 28 | P6.4 | I/O | General purpose digital I/O pin |
| | | | AINA4 | AI | ADC analog input 4 for sample-and-hold A |
| | | | CPN1 | AI | Analog comparator 1 negative input |
| 64 | 38 | 27 | P6.5 | I/O | General purpose digital I/O pin |
| | | | AINA5 | AI | ADC analog input 5 for sample-and-hold A |
| | | | CPP1 | AI | Analog comparator 1 positive input |
| 63 | 37 | - | P6.6 | I/O | General purpose digital I/O pin |
| | | | AINA6 | AI | ADC analog input 6 for sample-and-hold A |
| 62 | - | - | P6.7 | I/O | General purpose digital I/O pin |
| | | | AINA7 | AI | ADC analog input 7 for sample-and-hold A |
| 83 | 55 | - | P7.0 | I/O | General purpose digital I/O pin |
| | | | AINB0 | AI | ADC analog input 0 for sample-and-hold B |
| 82 | 54 | 40 | P7.1 | I/O | General purpose digital I/O pin |
| | | | AINB1 | AI | ADC analog input 1 for sample-and-hold B |
| 81 | 53 | 39 | P7.2 | I/O | General purpose digital I/O pin |
| | | | AINB2 | AI | ADC analog input 2 for sample-and-hold B |
| 80 | 52 | 38 | P7.3 | I/O | General purpose digital I/O pin |
| | | | AINB3 | AI | ADC analog input 3 for sample-and-hold B |
| 79 | 51 | - | P7.4 | I/O | General purpose digital I/O pin |
| | | | AINB4 | AI | ADC analog input 4 for sample-and-hold B |
| | | | CPN2 | AI | Analog comparator 2 negative input |
| 78 | 50 | 37 | P7.5 | I/O | General purpose digital I/O pin |
| | | | AINB5 | AI | ADC analog input 5 for sample-and-hold B |
| | | | CPP2 | AI | Analog comparator 2 positive input |



| Pin Number | | | Pin Name | Pin Type ^[1] | Description |
|------------|--------|--------|----------|-------------------------|--|
| 100-pin | 64-pin | 48-pin | | | |
| 77 | 49 | - | P7.6 | I/O | General purpose digital I/O pin |
| | | | AINB6 | AI | ADC analog input 6 for sample-and-hold B |
| 76 | - | - | P7.7 | I/O | General purpose digital I/O pin |
| | | | AINB7 | AI | ADC analog input 7 for sample-and-hold B |
| 72 | 46 | 34 | P8.0 | I/O | General purpose digital I/O pin |
| | | | OPP0 | AI | OP Amplifier 0 positive input |
| 71 | 45 | 33 | P8.1 | I/O | General purpose digital I/O pin |
| | | | OPN0 | AI | OP Amplifier 0 negative input |
| 70 | 44 | 32 | P8.2 | I/O | General purpose digital I/O pin |
| | | | OPO0 | AO | OP Amplifier 0 output |
| 85 | - | - | P8.3 | I/O | General purpose digital I/O pin |
| | | | CPN0 | AI | Analog comparator negative input pin |
| 84 | - | - | P8.4 | I/O | General purpose digital I/O pin |
| | | | CPP0 | AI | Analog comparator positive input pin |
| 91 | - | - | P8.5 | I/O | General purpose digital I/O pin |
| 59 | - | - | P8.6 | I/O | General purpose digital I/O pin |
| 58 | - | - | P8.7 | I/O | General purpose digital I/O pin |
| | | | CPO0 | O | Analog comparator output pin |
| 86 | 56 | 41 | P9.0 | I/O | General purpose digital I/O pin |
| | | | OPO1 | AO | OP Amplifier 1 output |
| 87 | 57 | 42 | P9.1 | I/O | General purpose digital I/O pin |
| | | | OPN1 | AI | OP Amplifier 1 negative input |
| 88 | 58 | 43 | P9.2 | I/O | General purpose digital I/O pin |
| | | | OPP1 | AI | OP Amplifier 1 positive input |
| 92 | - | - | P9.3 | I/O | General purpose digital I/O pin |
| | | | BKP11 | I | Brake input pin 1 of PWM Unit 1 |
| 98 | - | - | P9.4 | I/O | General purpose digital I/O pin |
| | | | SPI_CLK1 | I/O | SPI1 serial clock pin |
| 99 | - | - | P9.5 | I/O | General purpose digital I/O pin |
| | | | MISO1 | I/O | SPI1 MISO (Master In, Slave Out) pin |
| 100 | - | - | P9.6 | I/O | General purpose digital I/O pin |
| | | | MOSI1 | I/O | SPI1 MOSI (Master Out, Slave In) pin |
| 2 | 2 | - | P9.7 | I/O | General purpose digital I/O pin |

| Pin Number | | | Pin Name | Pin Type ⁽¹⁾ | Description |
|------------|--------|--------|----------|-------------------------|---------------------------------------|
| 100-pin | 64-pin | 48-pin | | | |
| | | | /SS1 | I/O | SPI1 slave select pin |
| 13 | 10 | 8 | PA.0 | I/O | General purpose digital I/O pin |
| | | | TX1 | O | Data transmitter output pin for UART1 |
| | | | I2CSDA | I/O | I2C data input/output pin |
| 12 | 9 | 7 | PA.1 | I/O | General purpose digital I/O pin |
| | | | RX1 | I | Data Receiver input pin for UART1 |
| | | | I2CSCL | I/O | I2C clock output pin |

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---------------------|---------|---------|------|
| DC Power Supply | VDD-VSS | -0.3 | +6.3 | V |
| Input Voltage | VIN | VSS-0.3 | VDD+0.3 | V |
| Oscillator Frequency | 1/t _{CLCL} | 4 | 24 | MHz |
| Operating Temperature | TA | -40 | 105 | °C |
| Storage Temperature | TST | -55 | +150 | °C |
| Maximum Current into VDD | | - | 120 | mA |
| Maximum Current out of VSS | | | 120 | mA |
| Maximum Current sunk by a I/O pin | | | 35 | mA |
| Maximum Current sourced by a I/O pin | | | 35 | mA |
| Maximum Current sunk by total I/O pins | | | 100 | mA |
| Maximum Current sourced by total I/O pins | | | 100 | mA |

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

6.2 DC Electrical Characteristics

| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS |
|--------------------------------------|---------------------------------------|---------------|------|------------------|------|--|
| | | MIN. | TYP. | MAX. | UNIT | |
| Operation voltage | V _{DD} | 2.5 | - | 5.5 | V | V _{DD} = 2.5V ~ 5.5V |
| Power Ground | V _{SS} / AV _{SS} | -0.3 | - | - | V | |
| LDO Output Voltage | V _{LDO} | 1.62 | 1.8 | 1.98 | V | V _{DD} ≥ 2.5V |
| Analog Operating Voltage | AV _{DD} | 2.5 | - | V _{DD} | V | |
| Analog Reference Voltage | V _{ref} | 1.2 | - | AV _{DD} | V | |
| Operating Current Normal Run Mode | I _{DD1} | - | - | 0.61F+8.1 | mA | V _{DD} = 5V, enable all IP and PLL, external XTAL |
| | I _{DD2} | - | - | 0.32F+7.7 | mA | V _{DD} = 5V, disable all IP and enable PLL, external XTAL |
| | I _{DD3} | - | - | 0.58F+8.1 | mA | V _{DD} = 3.3V, enable all IP and PLL, external XTAL |
| | I _{DD4} | - | - | 0.29F+7.7 | mA | V _{DD} = 3.3V, disable all IP and enable PLL, external XTAL |
| | I _{DD5} | - | - | 0.66F+0.4 | mA | V _{DD} = 5V, enable all IP and disable PLL, external XTAL |
| | I _{DD6} | - | - | 0.40F+0.2 | mA | V _{DD} = 5V, disable all IP and disable PLL, external XTAL |
| | I _{DD7} | - | - | 0.60F+0.4 | mA | V _{DD} = 3.3V, enable all IP and disable PLL, external XTAL |
| | I _{DD8} | - | - | 0.35F+0.2 | mA | V _{DD} = 3.3V disable all IP and disable PLL, external XTAL |

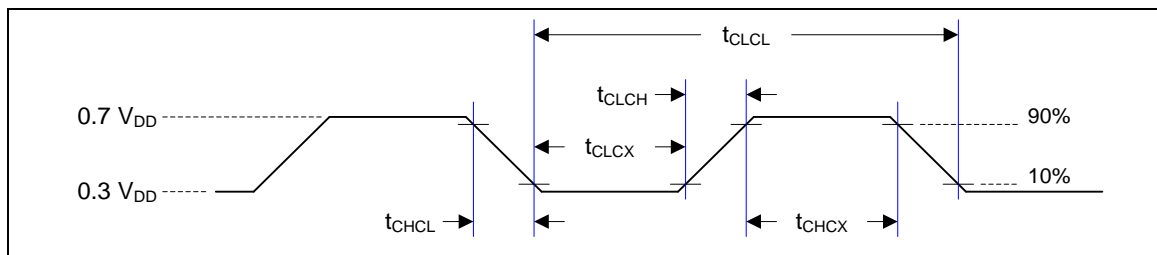
| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS |
|---|--------------------------------|---------------|------|-----------|------|--|
| | | MIN. | TYP. | MAX. | UNIT | |
| Operating Current Idle Mode | I _{IDLE1} | - | - | 0.39F+8.1 | mA | V _{DD} = 5V, enable all IP and PLL, external XTAL |
| | I _{IDLE2} | - | - | 0.09F+7.7 | mA | V _{DD} = 5V, disable all IP and enable PLL, external XTAL |
| | I _{IDLE3} | - | - | 0.37F+8.1 | mA | V _{DD} = 3.3V, enable all IP and PLL, external XTAL |
| | I _{IDLE4} | - | - | 0.08F+7.7 | mA | V _{DD} = 3.3V, disable all IP and enable PLL, external XTAL |
| | I _{IDLE5} | - | - | 0.43F+0.5 | mA | V _{DD} = 5V, enable all IP and disable PLL, external XTAL |
| | I _{IDLE6} | - | - | 0.18F+0.4 | mA | V _{DD} = 5V, disable all IP and disable PLL, external XTAL |
| | I _{IDLE7} | - | - | 0.38F+0.5 | mA | V _{DD} = 3.3V, enable all IP and disable PLL, external XTAL |
| | I _{IDLE8} | - | - | 0.13F+0.4 | mA | V _{DD} = 3.3V disable all IP and disable PLL, external XTAL |
| Standby Current Power-down Mode | I _{PWD} | - | - | 25 | μA | V _{DD} = 5.5V, No load @ Disable BOV function, 25°C |
| Logic 0 Input Current (Quasi-bidirectional mode) | I _{IL} | - | - | -75 | μA | |
| Input Leakage Current (input only) | I _{LK} | - | - | 2 | μA | |
| Logic 1 to 0 Transition Current (Quasi-bidirectional mode) | I _{TL} ^[3] | - | - | -660 | μA | V _{DD} = 5.5V, V _{IN} < 2.0V |
| Internal Pull-High Resistor of /RESET ^[1] | R _{RST} | 15 | - | - | kΩ | |

| PARAMETER | SYM. | SPECIFICATION | | | | TEST CONDITIONS |
|---|-----------|-----------------|-------------|-----------------|---------|------------------------------|
| | | MIN. | TYP. | MAX. | UNIT | |
| Input Low Voltage (TTL input) | V_{IL} | -0.3 | - | $0.2V_{DD}-0.1$ | V | |
| Input Low Voltage (Schmitt input) | V_{IL1} | -0.3 | | $0.3V_{DD}$ | V | |
| Input Low Voltage (/RESET, XTAL in) | V_{IL2} | -0.3 | | $0.15V_{DD}$ | V | |
| Input High Voltage (TTL input) | V_{IH} | $0.2V_{DD}+0.9$ | - | $V_{DD}+0.3$ | V | |
| Input High Voltage (Schmitt input, /RESET, XTAL in) | V_{IH1} | $0.7V_{DD}$ | - | $V_{DD}+0.3$ | V | |
| Hysteresis voltage of (Schmitt input) | V_{HY} | - | $0.2V_{DD}$ | - | V | |
| Source Current (Quasi-bidirectional Mode) | I_{OH} | -360 | - | - | μA | $V_{DD} = 4.5V, V_S = 2.4V$ |
| | | -60 | - | - | μA | $V_{DD} = 2.7V, V_S = 2.2V$ |
| | | -50 | - | - | μA | $V_{DD} = 2.5V, V_S = 2.0V$ |
| Source Current (Push-pull Mode) | I_{OH1} | -25 | - | - | mA | $V_{DD} = 4.5V, V_S = 2.4V$ |
| | | -4 | - | - | mA | $V_{DD} = 2.7V, V_S = 2.2V$ |
| | | -3 | - | - | mA | $V_{DD} = 2.5V, V_S = 2.0V$ |
| Sink Current (Quasi-bidirectional and Push-pull Mode) | I_{OL} | 16 | - | - | mA | $V_{DD} = 4.5V, V_S = 0.45V$ |
| | | 10 | - | - | mA | $V_{DD} = 2.7V, V_S = 0.45V$ |
| | | 9 | - | - | mA | $V_{DD} = 2.5V, V_S = 0.45V$ |

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. I/O pin can source a transition current when they are being externally driven from 1 to 0. In the condition of $V_{DD}=5.5V$, 5 μs the transition current reaches its maximum value when V_{IN} approximates to 2V.

6.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------|-----------------|-----------|------|------|------|------|
| t_{CHCX} | Clock High Time | | 10 | - | - | nS |
| t_{CLCX} | Clock Low Time | | 10 | - | - | nS |
| t_{CLCH} | Clock Rise Time | | 2 | - | 15 | nS |
| t_{CHCL} | Clock Fall Time | | 2 | - | 15 | nS |

6.3.1 External 4~24MHz Crystal

| PARAMETER | CONDITION | MIN. | TYP.. | MAX. | UNIT |
|----------------------------|-------------------------|------|-------|------|------|
| Operation Voltage V_{DD} | - | 2.5 | - | 5.5 | V |
| Temperature | - | -40 | - | 85 | °C |
| Operating Current | 12 MHz at $V_{DD} = 5V$ | - | 1 | - | mA |
| Clock Frequency | External crystal | 4 | | 24 | MHz |

6.3.1.1 Typical Crystal Application Circuits

| CRYSTAL | C1 | C2 | R |
|----------------|----------|----------|---------|
| 4 MHz ~ 24 MHz | 10~20 pF | 10~20 pF | without |

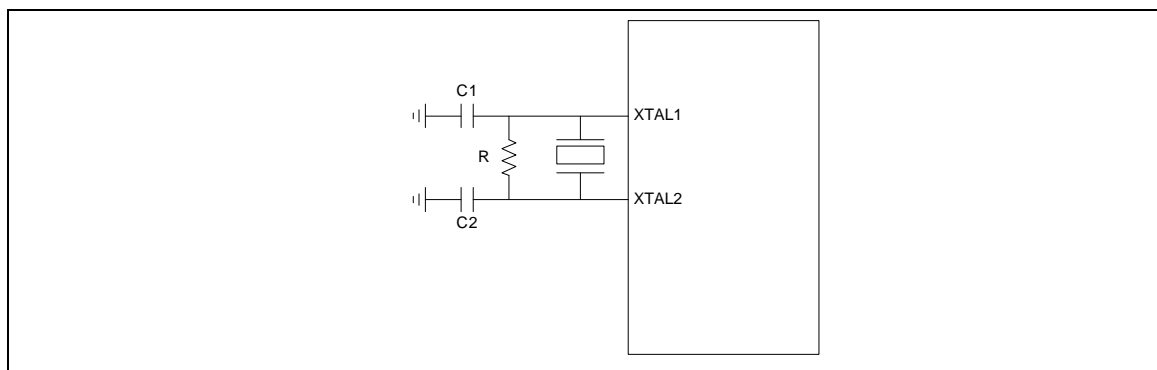


Figure 6-1 Typical Crystal Application Circuit

6.3.2 Internal 22.1184 MHz Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|----------------------------------|---|------|---------|------|------|
| Supply voltage | - | 2.5 | - | 5.5 | V |
| Frequency (After calibration) | - | - | 22.1184 | - | MHz |
| | +25°C; $V_{DD} = 5V$ | -1 | - | +1 | % |
| | -40 to +105°C; $V_{DD} = 2.5V \sim 5.5V$ | -2 | - | +2 | % |
| Operation Current | $V_{DD} = 5V$ | - | 500 | - | uA |

6.3.3 Internal 10 kHz Oscillator

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|--|---|------|------|------|------|
| Supply voltage | - | 2.5 | - | 5.5 | V |
| Center Frequency | - | - | 10 | - | kHz |
| Calibrated Internal Oscillator Frequency | +25°C; $V_{DD} = 5V$ | -30 | - | +30 | % |
| | -40°C ~ +85°C; $V_{DD} = 2.5V \sim 5.5V$ | -50 | - | +50 | % |

6.4 Analog Characteristics

6.4.1 Specification of 12-bit SARADC

| PARAMETER | SYMBOL | CONDITON | MIN. | TYP. | MAX. | UNIT |
|---------------------------------|-----------|-------------|------------|-------|-------|-------|
| Resolution | - | | 12 | | | Bit |
| Differential nonlinearity error | DNL | | - | -1~+2 | -1~+4 | LSB |
| Integral nonlinearity error | INL | | - | ±1.5 | ±4 | LSB |
| Offset error | EO | | - | +3 | +5 | LSB |
| Full scale error | EG | | - | -3 | -6 | LSB |
| Absolute error | EA | | | - | ±4 | |
| Monotonic | - | | Guaranteed | | | |
| ADC clock frequency | F_{ADC} | AVDD = 4.5V | - | - | 16 | MHz |
| | | AVDD = 2.5V | - | - | 8 | |
| Sample rate | F_S | AVDD = 4.5V | - | - | 800 | kps |
| | | AVDD = 2.5V | - | - | 400 | |
| Sample time | T_S | | - | 8 | - | Clock |
| Conversion time | T_{ADC} | | - | 12 | - | Clock |
| Supply voltage | AVDD | | 2.5 | - | 5.5 | V |
| VRFE voltage | VREF | | 2.0 | | AVDD | |
| Supply current | I_{DDA} | | - | 1.5 | - | mA |
| Reference current | I_{RFE} | | - | 1 | - | mA |
| Input voltage | V_{IN} | | 0 | - | VREF | V |
| Resistance | R_{IN} | | | 6 | | kΩ |
| Capacitance | C_{IN} | | - | 5 | - | pF |

6.4.2 Specification of LDO

| PARAMETER | MIN. | TYP. | MAX. | UNIT | NOTE |
|------------------------|------|------|------|------|------------------------|
| Input Voltage V_{DD} | 2.5 | | 5.5 | V | V_{DD} input voltage |
| Output Voltage | 1.62 | 1.8 | 1.98 | V | $V_{DD} > 2.5$ V |
| Operating Temperature | -40 | 25 | 105 | °C | |
| Cbp | - | 1 | - | μF | $R_{ESR} = 1 \Omega$ |

Note:

1. It is recommended that a 10 μF or higher capacitor and a 100 nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.
2. To ensure power stability, a 1 μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

6.4.3 Specification of Low Voltage Reset

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------------------|------------------------|------|------|------|--------------------|
| Operation Voltage | - | 0 | - | 5.5 | V |
| Quiescent Current | $AV_{DD}=5.5\text{ V}$ | - | 1 | 5 | μA |
| Operation Temperature | - | -40 | 25 | 105 | $^{\circ}\text{C}$ |
| Threshold Voltage | - | 1.6 | 2.0 | 2.4 | V |
| Hysteresis | - | 0 | 0 | 0 | V |

6.4.4 Specification of Brown-out Detector

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------|------------------------|------|------|------|--------------------|
| Operation Voltage | - | 0 | - | 5.5 | V |
| Temperature | - | -40 | 25 | 105 | $^{\circ}\text{C}$ |
| Quiescent Current | $AV_{DD}=5.5\text{ V}$ | - | - | 125 | μA |
| Brown-out Voltage | BOD_VL[1:0]=11 | 4.2 | 4.4 | 4.6 | V |
| | BOD_VL [1:0]=10 | 3.5 | 3.7 | 3.9 | V |
| | BOD_VL [1:0]=01 | 2.6 | 2.7 | 2.8 | V |
| | BOD_VL [1:0]=00 | 2.1 | 2.2 | 2.3 | V |
| Hysteresis | - | 30 | - | 150 | mV |

6.4.5 Specification of Power-On Reset (5V)

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------------------|---------------------------------|------|------|------|--------------------|
| Operation Temperature | - | -40 | 25 | 105 | $^{\circ}\text{C}$ |
| Reset Voltage | V+ | - | 2 | - | V |
| Quiescent Current | $V_{in} > \text{reset voltage}$ | - | 1 | - | nA |

6.4.6 Specification of Temperature Sensor

| PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|-------|------|-------|
| Operation Voltage ^[1] | | 2.5 | - | 5.5 | V |
| Operation Temperature | | -40 | - | 105 | °C |
| Current Consumption | | 6.4 | - | 10.5 | μA |
| Gain | | | -1.76 | | mV/°C |
| Offset Voltage | Temp=0 °C | | 720 | | mV |

6.4.7 Specification of Comparator

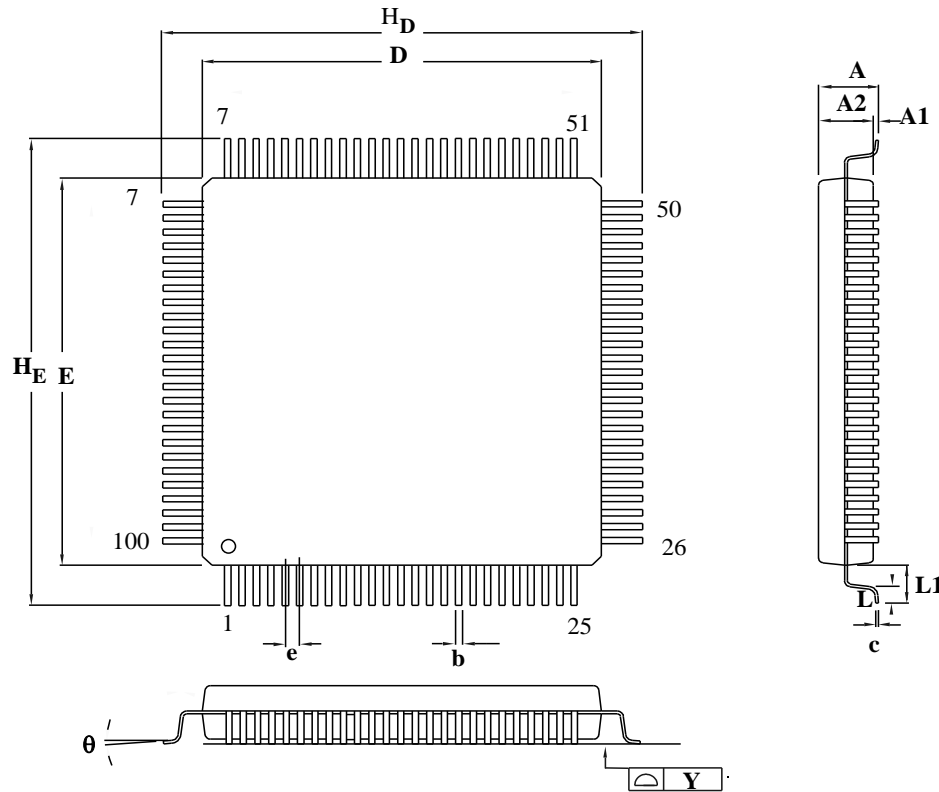
| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|------------------------------------|--|------|------|----------------------|------|
| Operation Voltage AV _{DD} | - | 2.5 | | 5.5 | V |
| Operation Temperature | - | -40 | 25 | 85 | °C |
| Operation Current | V _{DD} =3.0 V | - | 20 | 40 | μA |
| Input Offset Voltage | - | - | 5 | 15 | mV |
| Output Swing | - | 0.1 | - | V _{DD} -0.1 | V |
| Input Common Mode Range | - | 0.1 | - | V _{DD} -1.2 | V |
| DC Gain | - | - | 70 | - | dB |
| Propagation Delay | V _{CM} =1.2 V and V _{DIFF} =0.1 V | - | 200 | - | ns |
| Comparison Voltage | 20 mV at V _{CM} =1 V 50 mV at V _{CM} =0.1 V 50 mV at V _{CM} =V _{DD} -1.2 10 mV for non-hysteresis | 10 | 20 | - | mV |
| Hysteresis | V _{CM} =0.4 V ~ V _{DD} -1.2 V | - | ±10 | - | mV |
| Wake-up Time | C _{INP} =1.3 V C _{INN} =1.2 V | - | - | 2 | μs |

6.4.8 Specification of OP Amplifier

| PARAMETER | CONDITION | MIN. | TYP. | MAX. | UNIT |
|----------------------------|----------------------------------|------|------|---------|-------|
| AVDD | - | 3.0 | 3.3 | 5.5 | V |
| Input offset voltage | - | - | 2 | 5 | mV |
| Input offset average drift | - | - | - | 1 | uV/°C |
| Output swing | - | 0.1 | - | VDD-0.1 | V |
| Input common mode range | - | 0.1 | - | VDD-1.2 | V |
| DC gain | - | - | 80 | - | dB |
| Unity gain freq. | AVDD=5V | - | - | 5 | MHz |
| Phase margin | - | - | 50° | - | ° |
| PSRR+ | AVDD=5V | - | 90 | - | dB |
| CMRR | AVDD=5V | - | 90 | - | dB |
| Slew rate | AVDD=5V, RLOAD=33K, CLOAD=50p | 6.0 | - | - | V/us |
| Wake up time | - | - | - | 1 | us |
| Quiescent current | - | - | - | 2 | mA |

7 PACKAGE DIMENSIONS

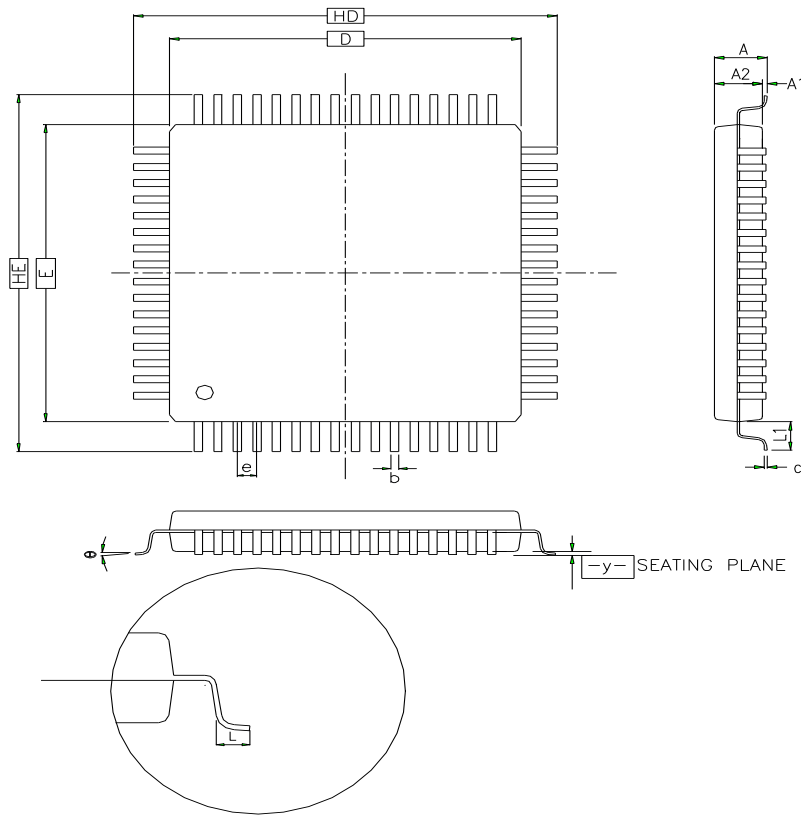
7.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

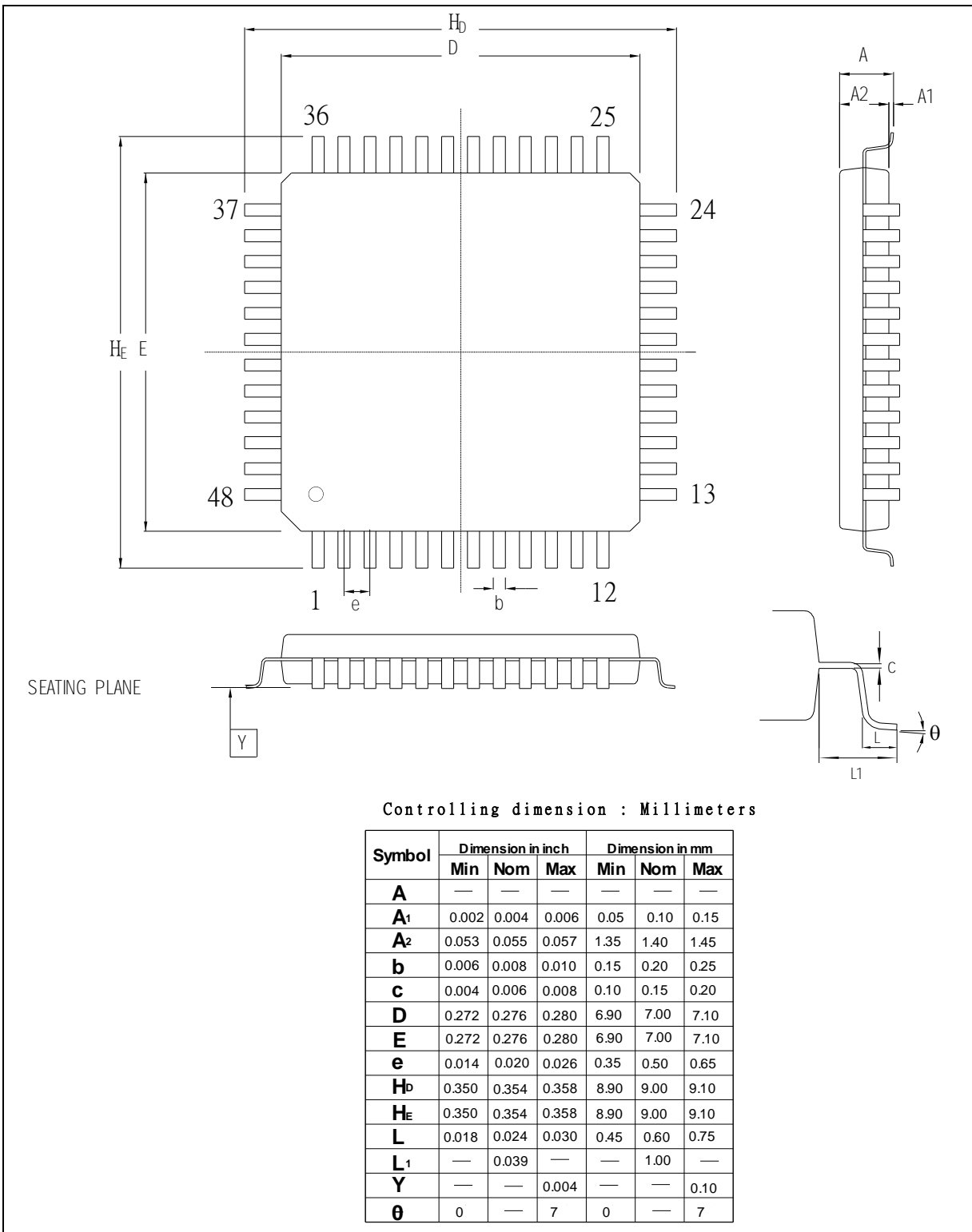
| Symbol | Dimension in inch | | | Dimension in mm | | |
|----------|-------------------|-------|-------|-----------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 0.063 | — | — | 1.60 |
| A1 | 0.002 | — | — | 0.05 | — | — |
| A | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| c | 0.004 | 0.006 | 0.008 | 0.10 | 0.15 | 0.20 |
| D | 0.547 | 0.551 | 0.556 | 13.90 | 14.00 | 14.10 |
| E | 0.547 | 0.551 | 0.556 | 13.90 | 14.00 | 14.10 |
| e | — | 0.020 | — | — | 0.50 | — |
| H_D | 0.622 | 0.630 | 0.638 | 15.80 | 16.00 | 16.20 |
| H_E | 0.622 | 0.630 | 0.638 | 15.80 | 16.00 | 16.20 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| L1 | — | 0.039 | — | — | 1.00 | — |
| y | — | — | 0.004 | — | — | 0.10 |
| θ | 0° | — | 7° | 0° | — | 7° |

7.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



| Symbol | Dimension in inch | | | Dimension in mm | | |
|----------------------|-------------------|-------|-------|-----------------|-------|------|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 0.063 | — | — | 1.60 |
| A₁ | 0.002 | — | 0.006 | 0.05 | — | 0.15 |
| A₂ | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.007 | 0.008 | 0.011 | 0.17 | 0.20 | 0.27 |
| c | 0.004 | — | 0.008 | 0.09 | — | 0.20 |
| D | — | 0.393 | — | — | 10.00 | — |
| E | — | 0.393 | — | — | 10.00 | — |
| e | — | 0.020 | — | — | 0.50 | — |
| H_D | — | 0.472 | — | — | 12.00 | — |
| H_E | — | 0.472 | — | — | 12.00 | — |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| L₁ | — | 0.039 | — | — | 1.00 | — |
| y | — | 0.004 | — | — | 0.10 | — |
| θ | 0 | 3.5 | 7 | 0 | 3.5 | 7 |

7.3 48L LQFP (7x7x1.4mm footprint 2.0mm)



8 REVISION HISTORY

| REVISION | DATE | PAGE | DESCRIPTION |
|----------|------------|------|---|
| V0.1 | 2011/8/30 | | Preliminary release. |
| V0.2 | 2012/03/20 | | 1. Synchronized to TRM V0.2 |
| V0.3 | 2012/10/08 | | 1. Update the part numbers with MT510, MT520 and MT530. |
| V0.4 | 2014/04/09 | | 1. Change part name from MT5xx to NM15xx. 2. Update description of features |
| V0.5 | 2014/06/19 | | 1. Update the diagrams of pin configuration |
| V0.6 | 2014/7/18 | | 1. Update the Specification of 12-bit SARADC |
| V0.7 | 2014/7/25 | | 1. Correct P7.4 and P7.5 about comparator input in Pin Description. |
| V0.8 | 2015/2/25 | | 1. Correct the content of LDROM size in chapter 2. |
| V0.9 | 2016/03/01 | | 1. Correct pin assignment of IC10~IC12. Modify chapter4 of part list, chapter5 of pin configuration |
| V0.9.3 | 2017/05/22 | | 1. Add new part of NM1521 LQFP64 |

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